UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,418	10/27/2003	Richard M. Barth	060809-0142-US	4481

38426 7590 10/27/2005

MORGAN LEWIS & BOCKIUS LLP/RAMBUS INC.
2 PALO ALTO SQUARE
3000 EL CAMINO REAL
PALO ALTO, CA 94306

EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/695,418	BARTH ET AL.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-24* is/are allowed.

6)☒ Claim(s) *2-8 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed July 28, 2005 in response to PTO Office Action mailed June 14, 2005. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 2-3, 9 and 25 have been amended. Claim 1 has been canceled. No claims have been added. As a result, claims 2-25 are now pending in this application.

Response to Arguments

3. Applicant's arguments filed July 28, 2005 have been fully considered but they are not persuasive. As to the Remarks, applicant asserted that:

Harriman is a poor basis for any 35 U.S.C. 103 rejection of the currently pending claims, because Harriman is not addressing the pipeline data bubble issue that is addressed by the present invention as defined by the pending claims.

Examiner respectfully traverses applicant's arguments for the following reasons.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Harriman is a poor basis for any 35 U.S.C. 103 rejection of the currently pending claims, because Harriman is

not addressing the pipeline data bubble issue that is addressed by the present invention as defined by the pending claims) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Butler and Harriman arbitrate between different types of memory addresses.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites the limitation "the data bus" in line 4. There is insufficient antecedent basis for this limitation in the claim. There is no previous mention of a data bus in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-4, 6 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645).

As per claim 2, Butler discloses a memory system, comprising:

a memory device (*system memory 206*; Fig. 2);

a data bus (*controller 304 is coupled to buffer memory 306 via an address/data bus*; col. 4, lines 30-31); and

a controller coupled to the memory device using the data bus (*controller 304 is coupled to buffer memory 306 via an address/data bus*; col. 4, lines 29-31), the controller including: an interface for receiving read, write commands (*controller arbitrates access to buffer 306 between reads, writes and memory refreshes*; col. 4, lines 34-36);

a buffer that temporarily stores write data corresponding to a first address in the memory device (*data received from the video source is written to the buffer 306 and from the buffer 306 to the system memory 206*; col. 4, lines 1-4); and

buffer control logic to transfer the write data corresponding to the first address from the buffer to the memory device in accordance with a current command (*FPGA 308 detects valid data and asserts a write enable signal to memory controller 304; memory controller 304 writes received data to SDRAM*

buffer 306; col. 4, lines 48-65; *data received from the video source is written to the buffer 306 and from the buffer 306 to the system memory 206*; col. 4, lines 1-4).

However, Butler does not specifically teach when the current command is a read command having an associated address that is the same as the first address, the controller delays issuance of the read command to the memory device as recited in the claim.

Harriman discloses delay granting of a read request when the read address corresponding to an address which is the same as the first address (col. 5, lines 1-6 and 24-27).

It would have been obvious to one of ordinary skill in the art, having the teachings of Butler and Harriman before him at the time the invention was made, to modify the system of Butler to include the controller performs delaying a read command when an address corresponding to the read command is the same as the first address because it would have provided needed coherency by reducing the average performance cost of the coherency scheme (col. 2, lines 27-28) as taught by Harriman.

Claim 3 is rejected using the same rationale as for the rejection of claim 2 above. Harriman further discloses the interface is also for receiving commands other than read and write commands (*controller arbitrates access to buffer 306 between reads, writes and memory refreshes*; col. 4, lines 34-36).

Claim 4 is rejected as per the rationale of the Harriman reference in claim 2 above.

As per claim 6, Butler discloses the buffer comprises a first in, first out (FIFO) buffer (col. 7, lines 5-9).

As per claim 25, Butler discloses a memory system, comprising:

a memory means (*system memory 206*; Fig. 2);

a communication means (*controller 304 is coupled to buffer memory 306 via an address/data bus*; col. 4, lines 30-31); and

a controller means coupled to the memory means using the communication means (*controller 304 is coupled to buffer memory 306 via an address/data bus*; col. 4,lines 29-31), wherein the controller means receives read, write commands (*controller arbitrates access to buffer 306 between reads, writes and memory refreshes*; col. 4, lines 34-36), temporarily stores write data corresponding to a first address in the memory means (*data received from the video source is written to the buffer 306 and from the buffer 306 to the system memory 206*; col. 4, lines 1-4), transfers the write data to the memory means in accordance with a current command (*FPGA 308 detects valid data and asserts a write enable signal to memory controller 304; memory controller 304 writes received data to SDRAM buffer 306*; col. 4, lines 48-61; *data received from the video source is written to the buffer 306 and from the buffer 306 to the system memory 206*; col. 4, lines 1-4).

However, Butler does not specifically teach when the current command is a read command having an associated address that is the same as the first address, the controller delays issuance of the read command to the memory device as recited in the claim.

Harriman discloses delay granting of a read request when the read address corresponding to an address which is the same as the first address (col. 5, lines 1-6 and 24-27).

It would have been obvious to one of ordinary skill in the art, having the teachings of Butler and Harriman before him at the time the invention was made, to modify the system of Butler to include the controller performs delaying a read command when an address corresponding to the read command is the same as the first address because it would have provided needed coherency by reducing the average performance cost of the coherency scheme (col. 2, lines 27-28) as taught by Harriman.

7. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645) and Lo et al (US 6,115,760).

As per claim 7, the combination of Butler and Harriman discloses the claimed invention as detailed above in the previous paragraphs. However, Butler and Harriman do not specifically teach the buffer control logic comprises a finite state machine as recited in the claim.

Lo discloses a buffer control logic comprises a finite state machine to effectively place a circuit stage in one of many possible operational modes (col. 7, lines 41-45).

Since the technology for implementing a control logic comprising a finite state machine was well known as evidenced by Lo, an artisan would have been motivated to implement this feature in the system of Butler and Harriman.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of Butler and Harriman to include a control logic comprising a finite state machine because it was well known to effectively place a circuit stage in one of many possible operational modes (col. 7, lines 41-45) as taught by Lo.

As per claim 8, the combination of Butler and Harriman discloses the claimed invention as detailed above in the previous paragraphs. However, Butler and Harriman do not specifically teach the finite state machine is implemented in a look-up table as recited in the claim.

Lo discloses a truth table for the implementation of a finite state machine of a control circuit to perform control selection by the control circuit (col. 8, lines 26-30).

Since the technology for implementing a finite state machine implemented in a look-up table was well known as evidenced by Lo, an artisan would have been motivated to implement this feature in the system of Butler and Harriman.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of Butler and Harriman to include a finite state machine implemented in a look-up table because it was well known provide a system does not require complex interface circuitry to perform of control selection by the control circuit (col. 2, lines 35-36, col. 8, lines 26-30) as taught by Lo.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Butler et al. (US 6,720,968) and Harriman (US 6,330,645) and Takada et al (US 6,633,961).

As per claim 5, the combination of Butler and Harriman discloses the claimed invention as detailed above in the previous paragraphs. However, Butler and Harriman do not specifically teach the write data is transferred from the buffer to the memory device if the controller is idle during a period of time as recited in the claim.

Takada discloses transferring write data from a buffer to a memory device if the controller is idle during a period of time [col. 26, lines 41-56] to provide reliable data insertion in a minimum delay time (col. 4, lines 66-67).

Since the technology for implementing transferring write data from a buffer to a memory device if the controller is idle during a period of time was well known as evidenced by Takada, an artisan would have been motivated to implement this feature in the system of Butler and Harriman.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the system of Butler and Harriman to include transferring write data from a buffer to a memory device if the controller is idle during a period of time because it was well known provide reliable data insertion in a minimum delay time (col. 4, lines 66-67) as taught by Takada.

Allowable Subject Matter

9. Claims 9-24 are allowed over the prior art of record.

10. The following is a statement of reasons for the indication of allowable subject matter:

As per claim 9, the prior art of record does not teach or suggest "a finite state machine has at least four states, a first state corresponding to an initial idle mode of operation, a second state corresponding to a write-once-to-the-buffer mode of operation, a third state corresponding to a wait mode of operation and a fourth state corresponding to a mite-twice-to-the-buffer mode of operation" in combination with the other elements set forth in the claimed invention.

Claims 10-24 are allowable as being dependent upon claim 9 and having additional allowable features therein.

Conclusion

11. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

12. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

October 25, 2005

PIERRE VITAL
PRIMARY EXAMINER